RAMAIAH
Institute of Technology

CURRICULUM

for the Academic year 2019 – 2020

(Revised Scheme)

ELECTRONICS AND COMMUNICATION ENGINEERING

III & IV SEMESTER B.E

RAMAIAH INSTITUTE OF TECHNOLOGY
(Autonomous Institute, Affiliated to VTU)
Bangalore – 560054.

About the Institute

Ramaiah Institute of Technology (RIT) (formerly known as M. S. Ramaiah Institute of Technology) is a self-financing institution established in Bangalore in the year 1962 by the industrialist and philanthropist, Late Dr. M S Ramaiah All engineering departments offering bachelor degree programs have been accredited by NBA. RIT is one of the few institutes with faculty student ratio of 1:15 and achieves excellent academic results. The institute is a participant of the Technical Education Quality Improvement Program (TEQIP), an initiative of the Government of India. All the departments are full with competent faculty, with 100% of them being postgraduates or doctorates. Some of the distinguished features of RIT are: State of the art laboratories, individual computing facility to all faculty members. All research departments are active with sponsored projects and more than 130 scholars are pursuing PhD. The Centre for Advanced Training and Continuing Education (CATCE), and Entrepreneurship Development Cell (EDC) have been set up on campus. RIT has a strong Placement and Training department with a committed team, a fully equipped Sports department, large air-conditioned library with over 80,000 books with subscription to more than 300 International and National Journals. The Digital Library subscribes to several online e-journals like IEEE, JET etc. RIT is a member of DELNET, and AICTE INDEST Consortium. RIT has a modern auditorium, several hi-tech conference halls, all air-conditioned with video conferencing facilities. It has excellent hostel facilities for boys and girls. RIT Alumni have distinguished themselves by occupying high positions in India and abroad and are in touch with the institute through an active Alumni Association. RIT obtained Academic Autonomy for all its UG and PG programs in the year 2007. As per the National Institutional Ranking Framework, MHRD, Government of India, Ramaiah Institute of Technology has achieved 64th rank in 2019 among the top 100 engineering colleges across India.

About the Department

The Department of Electronics and Communication was started in 1975 and has grown over the years in terms of stature and infrastructure. The department has well equipped simulation and electronic laboratories and is recognized as a research center under VTU. The department currently offers a B. E. program with an intake of 120, and two M. Tech programs, one in Digital Electronics and Communication, and one in VLSI Design and Embedded Systems, with intakes of 30 and 18 respectively. The department has a Center of Excellence in Food Technologies sponsored by VGST, Government of Karnataka. The department is equipped with numerous UG and PG labs, along with R & D facilities. Past and current research sponsoring agencies include DST, VTU, VGST and AICTE with funding amount worth Rs. 1 crore. The department has modern research ambitions to develop innovative solutions and products and to pursue various research activities focused towards national development in various advanced fields such as Signal Processing, Embedded Systems, Cognitive Sensors and RF Technology, Software Development and Mobile Technology.

Vision of the Institute

To be an Institution of International Eminence, renowned for imparting quality technical education, cutting edge research and innovation to meet global socio-economic needs

Mission of the Institute

RIT shall meet the global socio-economic needs through

- *Imparting quality technical education by nurturing a conducive learning environment through continuous improvement and customization*
- *Establishing research clusters in emerging areas in collaboration with globally reputed organizations*
- *Establishing innovative skills development, techno-entrepreneurial activities and consultancy for socio-economic needs*

Quality Policy

We at M. S. Ramaiah Institute of Technology strive to deliver comprehensive, continually enhanced, global quality technical and management education through an established Quality Management System complemented by the synergistic interaction of the stake holders concerned

Vision of the Department

To evolve into a department of national and international repute for excellence in education and cutting-edge research in the domain of Electronics and Communication Engineering

Mission of the Department

The department will continuously strive to

1. *Provide a world-class learning environment that caters to local and global technological and social requirements*
2. *Initiate research collaborations with academia and industries to perform cutting edge research leading to socio-technological innovations*
3. *Develop skills for pursuing innovation and entrepreneurial ventures for graduating engineers*

Program Educational Objectives (PEOs):

PEO1: *To train to be employed as successful professionals in a core area of their choice*

PEO2: *To participate in lifelong learning/ higher education efforts to emerge as expert researchers and technologists*

PEO3: *To develop their skills in ethical, professional, and managerial domains*

Program Outcomes (POs):

PO1: ***Engineering knowledge:*** *Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.*

PO2: ***Problem analysis:*** *Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences*.

PO3: ***Design/development of solutions:*** *Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.*

PO4: ***Conduct investigations of complex problems:*** *Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions*.

PO5: ***Modern tool usage:*** *Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.*

PO6: ***The engineer and society:*** *Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.*

PO7: ***Environment and sustainability:*** *Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.*

PO8: ***Ethics:*** *Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.*

PO9: ***Individual and team work:*** *Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.*

PO10: ***Communication:*** *Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.*

PO11: ***Project management and finance:*** *Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.*

PO12: ***Life-long learning:*** *Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.*

Program Specific Outcomes (PSOs):

PSO1: Circuit Design Concepts: *Apply basic and advanced electronics for implementing and evaluating various circuit configurations.*

PSO2: ***VLSI and Embedded Domain:*** *Demonstrate technical competency in the design and analysis of components in VLSI and Embedded domains.*

PSO3: ***Communication Theory and Practice:*** *Possess application level knowledge in theoretical and practical aspects required for the realization of complex communication systems.*

Semester wise Credit Breakdown for B E Degree Curriculum Batch 2018-22

Course Category \ Semester	First	Second	Third	Fourth	Fifth	Sixth	Seventh	Eighth	Total Credits
Basic Sciences (BSC)	9	8	4	4					**25**
Engineering Sciences (ESC)	11	10							**21**
Humanities, Social Sciences and Management (HSMC)		2			3		3		**8**
Professional Courses – Core (PCC)			21	21	15	11	10		**78**
Professional Courses– Elective (PEC)					3	3	6	3	**15**
Other Open Elective Courses (OEC)					3	3			**6**
Project Work (PROJ), Internship (IN)						4	1	17	**22**
Total Credits	**20**	**20**	**25**	**25**	**24**	**21**	**20**	**20**	**175**

SCHEME OF TEACHING III SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	EC31	Mathematics – III	BSC	3	1	0	4	5
2.	EC32	Analog Circuits	PCC	4	0	0	4	4
3.	EC33	Digital Design	PCC	4	0	0	4	4
4.	EC34	Data Structures using C++	ESC	3	1	0	4	5
5.	EC35	Signals and Systems	PCC	3	1	0	4	5
6.	EC36	Digital Electronic Measurements	PCC	3	0	0	3	3
7.	ECL37	Analog Circuits Laboratory	PCC	0	0	1	1	2
8.	ECL38	Digital Design Laboratory	PCC	0	0	1	1	2
9.	AM01*	Additional Mathematics - I	BSC	3	0	0	0	3
		Total		**23**	**3**	**2**	**25**	**33**

* Non Credit Mandatory Course L – Lecture (one hour) T - Tutorial (Two hours) P - Practical (Two hours)

Note:

1. The Non Credit Mandatory Course, Additional Mathematics – I is prescribed for III Semester Lateral Entry Diploma students admitted to III Semester of BE Program. The student shall register for this course along with other III semester courses. The students shall attend classes for the course during the semester and complete all formalities of attendance and CIE to appear for SEE. This Course shall not be considered for vertical progression, but completion of the course shall be mandatory for the award of the degree.
2. **AICTE Activity Points to be earned by students admitted to BE program (For more details refer to Chapter 6, AICTE, Activity Point Program, Model Internship Guidelines):**
   Every regular student, who is admitted to the 4 year degree program, is required to earn 100 activity points in addition to the total credits earned for the program. Students entering 4 years Degree Program through lateral entry are required to earn 75 activity points in addition to the total credits earned for the program. The activity points earned by the student shall be reflected on the students 8th Semester grade card. The activities to earn the points can be spread over the duration of the course. However, minimum prescribed duration should be fulfilled. Activity Points (non-credit) have no effect on SGPA/CGPA and shall not be considered for vertical progression.
   Incase student fail to earn the prescribed activity points, Eight semester Grade Card shall be issued only after earning the required activity Points. Students shall be eligible for the award of degree only after the release of the Eight Semester grade card.

IV SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	EC41	Mathematics – IV	BSC	3	1	0	4	5
2.	EC42	Linear Integrated Circuits	PCC	3	1	0	4	5
3.	EC43	Fields, Lines and Waves	PCC	3	1	0	4	5
4.	EC44	Digital Signal Processing	PCC	4	0	0	4	4
5.	EC45	Control Systems	PCC	3	1	0	4	5
6.	EC46	Microprocessors	PCC	3	0	0	3	3
7.	ECL47	DSP and Control Systems Laboratory	PCC	0	0	1	1	2
8.	ECL48	Microprocessors Laboratory	PCC	0	0	1	1	2
9.	AM02*	Additional Mathematics - II	BSC	3	0	0	0	3
		Total		**22**	**4**	**2**	**25**	**34**

* Non Credit Mandatory Course L – Lecture (one hour) T - Tutorial (Two hours) P - Practical (Two hours)

Note:

1. The Non Credit Mandatory Course, Additional Mathematics – II is prescribed for IV Semester Lateral Entry Diploma students admitted to BE Program. The student shall register for this course along with other IV semester courses. The students shall attend classes for the course during the semester and complete all formalities of attendance and CIE to appear for SEE. This Course shall not be considered for vertical progression, but completion of the course shall be mandatory for the award of the degree.
2. **AICTE Activity Points to be earned by students admitted to BE program (For more details refer to Chapter 6, AICTE, Activity Point Program, Model Internship Guidelines):**
   Every regular student, who is admitted to the 4 year degree program, is required to earn 100 activity points in addition to the total credits earned for the program. Students entering 4 years Degree Program through lateral entry are required to earn 75 activity points in addition to the total credits earned for the program. The activity points earned by the student shall be reflected on the students 8th Semester grade card. The activities to earn the points can be spread over the duration of the course. However, minimum prescribed duration should be fulfilled. Activity Points (non-credit) have no effect on SGPA/CGPA and shall not be considered for vertical progression.
   Incase student fail to earn the prescribed activity points, Eight semester Grade Card shall be issued only after earning the required activity Points. Students shall be eligible for the award of degree only after the release of the Eight Semester grade card.

III SEMESTER

ENGINEERING MATHEMATICS – III

Course Code: EC31 **Credits: 3:1:0**
Prerequisite: Calculus **Contact Hours: 70**
Course Coordinators: Dr. M. V. Govindaraju & Dr. M. Girinath Reddy

UNIT – I

Numerical Solution of Algebraic and Transcendental Equations: Method of false position, Newton - Raphson method.

Numerical solution of Ordinary Differential Equations: Taylor series method, Euler and modified Euler method, fourth order Runge-Kutta method.

Statistics: Curve fitting by the method of least squares, fitting linear, quadratic and geometric curves, correlation and regression.

UNIT – II

Linear Algebra: Elementary transformations on a matrix, Echelon form of a matrix, rank of a matrix, Consistency of system of linear equations, Gauss elimination and Gauss – Siedel method to solve system of linear equations, Eigen values and Eigen vectors of a matrix, Rayleigh power method to determine the dominant eigen value of a matrix, diagonalization of a matrix, solution of system of ODEs using matrix methods.

UNIT – III

Complex Variables – I: Functions of complex variables, Analytic function, Cauchy-Riemann equations in Cartesian and polar coordinates, Consequences of Cauchy-Riemann equations, Construction of analytic functions.

Transformations: Conformal transformation, Discussion of the transformations – $w = z^2, w = e^z$, and $w = z + \frac{a^2}{z}$ $(z \neq 0)$, Bilinear transformation.

UNIT – IV

Complex Variables – II: Complex integration, Cauchy theorem, Cauchy integral formula, Taylor and Laurent series (statements only), Singularities, Poles and residues, Cauchy residue theorem (statement only)

UNIT - V

Fourier Series: Convergence and divergence of infinite series of positive terms, Periodic function, Dirchlet conditions, Fourier series of periodic functions of period 2π and arbitrary period, Half range series, Fourier series of Periodic square wave, Half wave rectifier, Full wave rectifier, Saw-tooth wave with graphical representation, Practical harmonic analysis.

Textbooks:

1. Erwin Kreyszig, "Advanced Engineering Mathematics", Wiley Publication, 10th Edition, 2015.
2. B. S. Grewal, "Higher Engineering Mathematics", Khanna Publishers, 44th Edition, 2017.

References:

1. Glyn James, "Advanced Modern Engineering Mathematics", 4th Edition, Pearson Education, 2010.
2. Dennis G. Zill, Michael R. Cullen, "Advanced Engineering Mathematics", 3rd Edition, Jones and Barlett Publishers Inc., 2009.
3. Dennis G. Zill and Patric D. Shanahan, "A First Course in Complex Analysis with Applications", 2nd Edition, Jones and Bartlett Publishers, 2009.

Course Outcomes (COs):

1. Apply numerical techniques to solve engineering problems and fit a least squares curve to the given data. (POs – 1, 2, PSOs – 1, 3)
2. Test the system of linear equations for consistency and solve system of ODEs using matrix methods. (POs – 1, 2, PSOs – 1, 3)
3. Examine and construct analytic functions. (POs – 1, 2, PSOs – 1, 3)
4. Classify singularities of complex functions and evaluate complex integrals. (POs – 1, 2, PSOs – 1, 3)
5. Construct Fourier series expansion of a function/tabulated data. (POs – 1, 2, PSOs – 1, 3)

ANALOG CIRCUITS

Subject Code: EC32 **Credits: 4:0:0**
Prerequisite: Basic Electronics **Contact Hours: 56**
Course Coordinator: Dr. Lakshmi Shrinivasan

UNIT – I

Voltage and Current Laws: Kirchoff's Laws, Single Loop and Node-Pair Circuits, Connected Independent Sources, Voltage and Current Division.

Circuit Analysis: Nodal and Mesh Analysis, Super Node, Super Mesh, Delta-Wye Conversion.

UNIT – II

Circuit Analysis: Linearity, Superposition, Reciprocity, Thevenin's, Norton's and Maximum Power Transfer Theorems, Source Transformation.

Sinusoidal Steady-State Analysis: Forced Response, Complex Forcing Function, Phasor relationships for R, L and C, Impedances and Admittances in Nodal and Mesh Analysis, Superposition, Source Transformations, Thevenin's Theorem.

UNIT – III

BJT Small Signal Analysis: Two-port devices and hybrid model, Analysis of a transistor amplifier circuit using h-parameters (CE Configuration only), unbypassed CE amplifier, Miller's theorem, practical applications.

Feedback Amplifiers: Feedback concept, advantages of Negative feedback, Transfer gain with feedback, Loop gain, General characteristics of negative feedback amplifiers, Feedback amplifier topologies, effect of negative feedback on input and output resistance in voltage series feedback amplifier, effect of negative feedback on amplifier bandwidth.

UNIT – IV

Power Amplifiers: Classification of power amplifiers, Class A large signal amplifiers, Second harmonic distortion, conversion efficiency, power output, Transformer – Coupled audio power amplifier, Push – Pull amplifiers, Advantages of a Push–Pull system, Class B amplifiers, Complementary – Symmetry Circuits, Class AB operation, Class C and Class D amplifier, power transistor heat sink, thermal analogy of a power transistor.

UNIT – V

MOSFET as an Amplifier and a Switch: The I_D-V_{DS} characteristics for n-channel EMOSFET, large signal operation – transfer characteristic, operation as a switch, MOSFET circuits at DC, biasing in MOS amplifiers.

MOSFET Small Signal Operation and Models: Small signal equivalent circuit model, the transconductance g_m, T equivalent circuit model, common source amplifier, high frequency model of MOSFET, unity gain frequency, frequency response – low frequency, mid-band and high frequency analysis of common source amplifier.

Textbooks:

1. Robert L. Boylestad, Louis Nashelsky**,** "Electronic Devices and Circuit Theory", 11th Edition, PHI, 2014.
2. Adel S. Sedra, Kenneth C. Smith, "Micro-Electronic Circuits", 7th Edition, Oxford University Press, 2015.
3. C. K. Alexander, M. N. O. Sadiku, "Fundamentals of Electric Circuits", 3rd Edition, Tata McGraw Hill, 2008.

Reference:

1. Jacob Millman, Christos C Halkias, Satyabrata Jit, "Millman's Electronic Devices and Circuits", 2nd Edition, Tata McGraw Hill, 2007.

Course Outcomes (COs):

1. Employ nodal and mesh analysis techniques to various electric circuits. (POs – 1, 2, PSO – 1)
2. Apply network theorems to simplify electrical circuits. (POs – 1, 2, 5, PSO – 1)
3. Analyze BJT hybrid model, its significance in feedback amplifier circuits.(POs – 1, 2, 3, 12, PSO – 1)
4. Illustrate the importance of power amplifiers in analog circuit design. (POs – 1, 2, 4, 12, PSO – 1)
5. Interpret the low and high frequency response of a common source MOS amplifier. (POs – 1, 2, 4, PSO – 1)

DIGITAL DESIGN

Course Code: EC33 **Credits: 4:0:0**
Pre requisites: Basic Electronics **Contact Hours: 56**
Course Coordinator: Dr. V. Anandi

UNIT – I

Logic Simplification: SOP and POS forms, Canonical forms, Integrated circuits, Gate-Level Minimization: map method, Karnaugh maps – up to 4 variables, don't care, NAND and NOR implementation, Multilevel NAND / NOR Circuits.

Combinational Logic: Code conversion, binary adder, Carry propagation, binary subtractor, Decimal adder: BCD Adder, Binary multiplier, Magnitude comparator, Decoders, Logic implementation using decoders, Priority Encoder, Multiplexer, implementing Boolean function with a multiplexer, Three state gates.

UNIT – II

Hardware Description Language: Module Declaration, Gate Delays, User-Defined Primitives, HDL models of combinational circuits: Dataflow Modeling: two-to-one-line multiplexer, two-to-four-line decoder, four-bit comparator Gate-Level Modeling: two-to-four-line decoder, Hierarchical description of a four-bit adder, Three state gates.

Behavioral Modeling: Two-to-one-line multiplexer, four-to-one line multiplexer, writing simple test bench.

UNIT – III

Sequential Circuits: Storage elements: Latches: SR Latch, D Latch, flip-flops, Edge-Triggered D flip flop, other flip flops, characteristic tables, characteristic equations, direct inputs, Mealy and Moore models of FSM.

Registers and Counters: Registers, register with parallel load, universal shift register, binary ripple counter, BCD ripple counter, Synchronous counters: binary counter, up–down binary counter, counter with unused states, Ring counter, Johnson counter.

UNIT – IV

Synthesizable HDL models of Sequential Circuits: Behavioral modeling, HDL models of flip flops and latches, State diagram based HDL models: Mealy machine – Zero detectors.
HDL for Registers and Counters: Behavioral description of a 4-bit universal shift register, Structural description of a 4-bit universal shift register.

UNIT – V

Memory and Programmable Logic: Introduction, Random access memory, Read only memory, Programmable Logic Array, Programmable Array Logic, Memory description in HDL, RTL in HDL, Logic synthesis.

Textbook:

1. M. Morris Mano, Michael D. Ciletti , "Digital Design: with an Introduction to Verilog HDL", 5th Edition, Pearson Education, 2013.

References:

1. Michael D Ciletti , "Advanced Digital Design with Verilog HDL", 2nd Edition, Pearson Education, 2018.
2. Samir Palnitkar, "Verilog HDL – A guide to Digital Design and Synthesis", 2nd Edition Prentice Hall, 2010.

Course Outcomes (COs):

1. Recall the basics of digital design, and implement modular combinational designs. (POs – 1, 2, 3, PSO – 2)
2. Design, apply and test combinational circuits in HDL to verify the functionality. (POs – 1, 3, 4, 5, 8, PSO – 2)
3. Design and analyze sequential circuits. (POs – 1, 2, 3, PSO – 2)
4. Implement sequential circuits and test using test benches. (POs – 1, 3, 4, 5, 8, PSO – 2)
5. Justify the usage of EDA tools in logic synthesis with design tradeoffs. (POs – 1, 2, 3, 4, PSO – 2)

DATA STRUCTURES USING C++

Subject Code: EC34 **Credits: 3:1:0**
Prerequisite: Fundamentals of Computing **Contact Hours: 70**
Course Coordinator: Dr. K. Indira

UNIT – I

Classes and Objects: Introduction to OOPs, Objects as data types, Constructors, Destructors.

Arrays: Arrays as class member data, passing arrays, arrays of objects.

Operator Overloading, Friend Functions: Overloading of unary operators, binary operators, Friend functions.

UNIT – II

Pointers: Pointers and arrays, pointers and functions, memory management, pointers to objects.

Inheritance and Polymorphism: Inheritance, Types of Inheritances, Derived Class and Base Class, Overriding member functions, Scope resolution, Virtual Functions, Pure Virtual Functions.

UNIT – III

Stacks: Definition, representation, basic operations of stack (PUSH and POP) and its implementation, Applications of Stack: Conversion from Infix to Postfix, Evaluation of Postfix expression.

Queues: Definition, representation, primitive operations of queue and its implementation, Circular queues and Priority queues.

UNIT – IV

Linked Lists: Representation and implementation of operations (Insertion, Deletion and Search) of Singly, Doubly and Circular Linked Lists.

Applications: Implementation of stack and queue using lists.

Trees: Basic terminologies of binary trees, Binary tree traversal and its operations, Binary search trees.

UNIT – V

Graphs: Basic concepts, operations (insert and delete vertex, add and delete edge), traverse graph (Depth-first traversal), Graph storage structures (Adjacency matrix), Networks: minimum spanning tree (Prim's algorithm), shortest path algorithm (Dijkstra's).

Sorting and Searching: Sort concepts, selection sort (straight selection sort), insertion sort (straight selection sort), Quick sort, Merge sort, searching (sequential and binary search).

Tutorials: List of laboratory programs:
Introduction to C++ Programming**,** Class, Arrays of objects and objects as arguments**,** Friend functions, Constructors, Inheritance, Multiple Inheritance, Virtual functions**,** Stacks, Queues, Linked Lists, Trees, Graphs, Sorting and Searching.

Textbooks:

1. Robert Lafore, "Introduction to OOPs with C++", 4th Edition, Sams Publishing, 2001.
2. E. Balaguruswamy, "Object Oriented Programming with C++", 4th Edition, Tata McGraw Hill, 2011.
3. D. S. Malik, "Data Structures using C++", Indian Edition, Cengage Learning, 2003.

Reference:

1. Sourav Sahay, "Object Oriented Programming Using C++", 2nd Edition, Oxford University Press, 2013.

Course Outcomes (COs):

1. Employ overloading concepts to overload built in operators. (POs – 1, 2, 3, 5, 12, PSO – 2)
2. Apply the concept of inheritance in solving real world problems. (POs – 1, 2, 3, 5, 12, PSO – 2)
3. Implement stack and queue data structures and its applications. (POs –1, 2, 3, 5, 12, PSO – 2)
4. Develop various types of linked lists and trees. (POs – 1, 2, 3, 5, 12, PSO – 2)
5. Analyze algorithms to solve real world problems using graphs, sorting and searching techniques (POs – 1, 2, 3, 5, 12, PSO – 2)

SIGNALS AND SYSTEMS

Course Code: EC35 **Credits: 3:1:0**
Prerequisites: Engineering Mathematics **Contact Hours: 70**
Course Coordinator: Dr. Maya V Karki

UNIT – I

Introduction to Signals and Systems: Continuous time (CT) and Discrete time (DT) signals, transformations of the independent variable, Exponential and Sinusoidal signals, unit impulse and step functions, CT and DT systems, basic system properties.

UNIT – II

LTI Systems: Discrete time LTI systems, continuous time LTI systems, properties of LTI systems, causal LTI systems described by differential and difference equations, Block diagram representation of systems.

UNIT – III

Fourier Transform: Representation of aperiodic signals, Fourier Transform of periodic signals, properties of CTFT: Linearity, time shifting, conjugation and conjugate symmetry, differentiation and integration, time and frequency scaling, duality, Parseval's relation, convolution, multiplication, Representation of aperiodic signals by DTFT, DTFT of periodic signals.

UNIT – IV

Z Transform: Z transform, ROC of Z transform, inverse Z transform (partial fraction and power series only), properties of Z transform: Linearity, time shifting, scaling in the Z domain, time reversal, time expansion.

UNIT – V

Analysis using Z transform and Unilateral Z transform: Conjugation, convolution, differentiation in Z domain, initial value theorem, Analysis and characterization of LTI system using Z transform, system function algebraic representations, unilateral Z transform.

Textbook:

1. Alan V. Oppenheim, Alan S. Wilsky with S. Hamid Nawab, "Signals and Systems", 2nd Edition, PHI Publications, 2014.

References:

1. Simon Haykin, Barry Van Veen, "Signals and Systems", 2nd Edition, John Wiley & Sons, 2007.
2. M. J. Roberts, "Signals and Systems – Analysis using Transform Methods and MATLAB", 3rd Edition, TMH Publications, 2017.

Course Outcomes (COs):

1. Classify and analyze continuous, discrete time signals and systems. (POs – 1, 2, 9, PSO – 3)
2. Compute the response of a system using convolution. (POs – 1, 2, 9, PSO – 3)
3. Analyze the system by difference and differential equations. (POs – 1, 2, 3, 9, PSO – 3)
4. Employ Fourier transform to analyze signals and systems. (POs – 1, 2, 3, 9, PSO – 3)
5. Apply z transform and analyze signals and systems. (POs – 1, 2, 3, 9, PSO – 3)

DIGITAL ELECTRONIC MEASUREMENTS

Course Code: EC36 **Credits: 3:0:0**
Prerequisites: Basic Electronics **Contact Hours: 42**
Course Coordinator: Mrs. Punya Prabha V

UNIT – I

Measurement and Error: Definitions, Accuracy, Precision, Resolution, significant figures, Types of errors.

Voltmeters and Multimeters: Introduction, Basic meter as a DC voltmeter, DC voltmeter, Multi-range voltmeter, loading AC voltmeter using rectifiers, True RMS voltmeter, Multimeter.

Ammeters: DC Ammeter, Multi-range Ammeter, Ayrton Shunt.

UNIT – II

Digital Voltmeters: Introduction, RAMP technique, Dual slope integrating type DVM, Successive approximations, 3 1/2 digit, Resolution and sensitivity of digital meters, general specifications of DVM.

Digital Instruments: Digital tachometer, Digital PH meter, Digital phase meter, Frequency measurement, universal counter, Digital L, C and R measurements.

UNIT – III

Oscilloscopes: Fixed and variable AF oscillator, Basic principles, CRT features, Block diagram of oscilloscope, Simple CRO, Measurement of frequency by Lissajous method.

Special Oscilloscopes: Sampling oscilloscope, Digital read out oscilloscope, Digital storage oscilloscope.

Signal Generators: Arbitrary waveform generators (AWG), Key characteristics of digital signal generators, Standard signal generator, Laboratory type signal generator, Function generator.

UNIT – IV

Bridges: Introduction, Wheatstone's bridge, Kelvin's Bridge, AC bridges, Capacitance Comparison Bridge, Inductance Comparison Bridge, Maxwell's bridge, Wien's bridge.

Digital Spectrum Analyzer: Principle of working and its applications.

Recorders: Digital data recording, Objectives and requirements of recording data, Recorder selection and specifications.

UNIT – V

Digital Transducers: Optical encoders, Shaft (spatial) encoders.

Data Acquisition System: Objectives of DAS, Elements of DAS.

Digital Controllers: Direct digital and computer supervisory control, Digital process controllers

Data loggers: Basic operations.

Textbooks:

1. H. S. Kalsi, "Electronic Instrumentation", 3rd Edition, TMH, Seventh reprint, 2012.
2. David A. Bell, "Electronic Instrumentation and Measurements", 2nd Edition, PHI, 2009.

Reference:

1. Albert D. Helfrick, William D. Cooper, "Modern Electronic Instrumentation and Measurement Techniques", US Edition, PHI, 2012.

Course Outcomes (COs):

1. Employ the concept of different types of errors in the study of performance of various electronic instrumentation systems. (POs – 1, 2, PSO – 1)
2. Apply the concepts of basic principles of working of different electronic instruments. (POs – 1, 2, PSO – 1)
3. Illustrate design and testing of different circuits and systems, using suitable instruments. (POs – 1, 2, PSO – 1)
4. Select the instruments for observing different parameters. (POs – 1, 2, PSO – 1)
5. Demonstrate the use of data acquisition systems and digital process controllers in various industrial and electronics applications. (POs – 1, 2, 3, PSO – 1)

ANALOG CIRCUITS LABORATORY

Course Code: ECL36 **Credits: 0:0:1**
Prerequisite: Basic Electronics **Contact Sessions: 14**
Coordinator: Dr. Lakshmi Shrinivasan

LIST OF EXPERIMENTS

Hardware Experiments

1. Verification of Thevenin's theorem and Maximum Power Transfer Theorem
2. Study the input output characteristics of BJT CE amplifier and determine the h-parameters
3. Design and test a BJT RC coupled amplifier and plot the frequency response
4. Study of drain and transfer characteristics of n-channel MOSFET
5. Design and test RC phase shift oscillators
6. Design and test power amplifiers
   (i) Class A transformer coupled audio power amplifier
   (ii) Class B Push Pull power amplifier

Simulation Experiments

7. Verification of Superposition and Norton's Theorem
8. Design and test Bridge Rectifier with and without C filter
9. Design and test diode clipping and clamping circuits
10. Design and test RF oscillators (i) Hartley (ii) Colpitts
11. Design and test a FET RC coupled amplifier and plot the frequency response
12. Design a voltage series feedback amplifier. Compare the parameters with and without feedback.

Textbooks:

1. Robert L. Boylestad, Louis Nashelsky**,** "Electronic Devices and Circuit Theory", 11th Edition, PHI, 2015.
2. Adel S. Sedra, Kenneth C. Smith, "Micro-Electronic Circuits", 7th Edition, Oxford University Press, 2014.

Course Outcomes (COs):

1. Analyze network theorems using hardware and software. (POs – 1, 2, 3, 5, 8, 9, 10, PSO – 1)
2. Design amplifier circuits using BJT and FET devices. (POs – 1, 2, 3, 5, 8, 10, PSO – 1)
3. Implement diode clipping, clamping and rectifier circuits using software tool. (POs – 1, 2, 3, 5, 8, 9, 10, PSO – 1)
4. Analyze oscillator circuits using BJT in hardware and software. (POs – 1, 2, 3, 5, 8, 9, 10, PSO – 1)
5. Design power amplifier circuits. (POs – 1, 2, 3, 5, 8, 9, 10, PSO – 1)

DIGITAL DESIGN LABORATORY

Course Code: ECL36 **Credits: 0:0:1**
Prerequisite: Basic Electronics **Contact Sessions: 14**
Coordinator: Dr. V. Anandi

LIST OF EXPERIMENTS

The following experiments are realized using ICs and simulation done using Xilinx tools.

1. Logic gates
   (i) Realizing basic gates using universal NAND gates
   (ii) Implement the Boolean function using NOR gate and verify the truth table
2. Combinational circuits
   (i) Combinational circuit design
   (ii) Parity generator
   (iii) Gray code to binary converter
3. Decoder Implementation
   (i) 74155 decoder IC and external NAND gates
   (ii) BCD to seven segment decoder
4. HDL: Gate level modeling
   (i) Realization of combinational circuits
   (ii) Simple circuits with test bench
   (iii) 3 bit majority logic function
   (iv) 2-4 line decoder
   (v) Mux with tri-state gates
5. Multiplexers and Demultiplexers
   (i) IC 74153 – Implementing functions using mux
   (ii) Full adder with mux
   (iii) IC 74139 – Demultiplexer
6. HDL: Data flow modeling and test bench
   (i) BCD to Excess 3 converter
   (ii) Realization of 4:1 mux using conditional operator with test bench
   (iii) 4 bit adder
7. Adders
   (i) Adder – Subtractor using IC 7483
   (ii) Magnitude Comparator
8. HDL: Structural modeling with test bench
   (i) Realization of 16:1 mux using 4:1 mux hierarchical model
   (ii) Realization of 4 bit ripple carry adder using full adders
9. Flip flops (IC 7474/7476)
   (i) D Latch
   (ii) Master – Slave flip flop

10. Counters (IC 7476 and external gates)
    (i) Ripple counter using IC 7476
    (ii) Asynchronous decade counter using IC 7490
    (iii) Presettable counters (74192/193)
    (iv) Synchronous Counter
11. Behavioral modeling
    (i) 3:8 encoder with enable (with and without priority)
    (ii) JK flip flop
    (iii) D -type positive-edge-triggered flip-flop with asynchronous and direct inputs
    (iv) 4-bit BCD counter with asynchronous reset
    (v) Gray Counter
    (vi) any sequence Counter
12. Shift registers (IC 74195)
    (i) Left/Right Shift register
    (ii) Ring Counter/Feedback Shift Register
    (iii) HDL: shift register with parallel load
    (iv) Sequence detector
13. Programming RAM using IC 6116

Textbook:

1. M. Morris Mano, Michael D. Ciletti , "Digital Design: with an Introduction to Verilog HDL", 5th Edition, Pearson Education, 2013.

References:

1. Michael D Ciletti , "Advanced Digital Design with Verilog HDL", 2nd Edition, Pearson Education, 2018.
2. Samir Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", 2nd Edition, Prentice Hall, 2010.

Course Outcomes (COs):

1. Design combinational logic circuits using gates and MSI ICs. (POs – 1, 2, 9. PSO – 2)
2. Employ digital design tools for HDL simulation and test combinational circuits to verify the functionality. (POs – 1, 3, 4, 5, 9, 10, 12. PSO – 2)
3. Implement sequential logic circuits using MSI ICs. (POs – 1, 2, 3, 9. PSO – 2)
4. Design, simulate and test sequential logic circuits in behavioral modeling of HDL. (POs – 1, 2, 3, 9, PSO – 2)
5. Verify the operation of FSM. (POs – 1, 2, 3, 9. PSO – 2)

IV SEMESTER

ENGINEERING MATHEMATICS – IV

Course Code: EC41 **Credits: 3:1:0**
Prerequisite: Calculus & Probability **Contact Hours: 70**
Coordinator: Dr. M. V. Govindaraju & Dr. M. Girinath Reddy

UNIT – I

Finite Differences and Interpolation: Forward and backward differences, Interpolation, Newton-Gregory forward and backward interpolation formulae, Lagrange's interpolation formula and Newton's divided difference interpolation formula (no proof).

Numerical Differentiation and Numerical Integration: Derivatives using Newton-Gregory forward and backward interpolation formulae, Newton-Cotes quadrature formula, Trapezoidal rule, Simpson's $1/3^{rd}$ rule, Simpson's $3/8^{th}$ rule.

UNIT – II

Fourier Transforms: Infinite Fourier transform, Infinite Fourier sine and cosine transforms, Properties, Inverse transform, Convolution theorem, Parseval's identity (statements only), Fourier transform of rectangular pulse with graphical representation and its output discussion, Continuous Fourier spectra – example and physical interpretation.

Z-Transforms: Definition, standard Z-transforms, Single sided and double sided, Linearity property, Damping rule, Shifting property, Initial and final value theorem, Convergence of Z-transforms, Inverse Z-transform, Convolution theorem and problems, Application of Z-transforms to solve difference equations.

UNIT – III

Random Variables: Random Variables (Discrete and Continuous), Probability density function, Cumulative distribution function, Mean, Variance, Moment generating function.

Probability Distributions: Binomial and Poisson distributions, Uniform distribution, Exponential distribution, Gamma distribution, Normal distribution.

UNIT – IV

Joint Probability Distribution: Joint probability distribution (both discrete and continuous), conditional probability, conditional expectation.
Stochastic Processes: Introduction, Classification of stochastic processes, discrete time processes, Stationarity, Ergodicity, Autocorrelation, Power spectral density.

Markov Chain: Probability Vectors, Stochastic matrices, Regular stochastic matrices, Markov chains, Higher transition probabilities, Stationary distribution of regular Markov chains and absorbing states, Markov and Poisson processes.

UNIT – V

Series Solution of ODEs and Special Functions: Series solution, Frobenius method, Series solution of Bessel differential equation leading to Bessel function of first kind, Orthogonality of Bessel functions, Series solution of Legendre differential equation leading to Legendre polynomials, Rodrigues's formula**.**

Textbooks:

1. R. E. Walpole, R. H. Myers, R. S. L. Myers and K. Ye, "Probability and Statistics for Engineers and Scientists", 9th Edition, Pearson Education, Delhi, 2012.
2. B. S. Grewal, "Higher Engineering Mathematics", 44th Edition, Khanna Publishers, 2017.

References:

1. Erwin Kreyszig, "Advanced Engineering Mathematics", 10th Edition, Wiley Publication, 2015.
2. Glyn James, "Advanced Modern Engineering Mathematics", 4th Edition, Pearson Education, 2010.
3. Kishor S. Trivedi, "Probability & Statistics with Reliability, Queuing and Computer Science Applications", 2nd Edition, John Wiley & Sons, 2008.

Course Outcomes (COs):

1. Find functional values, derivatives, areas and volumes numerically from a given data. (POs – 1, 2, PSOs – 1, 3)
2. Evaluate Fourier transforms and use Z-transforms to solve difference equations. (POs – 1, 2, PSOs – 1, 3)
3. Analyze the given random data and its probability distributions. (POs – 1, 2, PSOs – 1, 3)
4. Determine the parameters of stationary random processes and use Markov chain in prediction of future events. (POs – 1, 2, PSOs – 1, 3)
5. Obtain the series solution of ordinary differential equations. (POs – 1, 2, PSOs – 1, 3)

LINEAR INTEGRATED CIRCUITS

Course Code: EC42 **Credits: 3:1:0**
Prerequisite: Analog Electronics **Contact Hours: 70**
Course Coordinator: Mrs. H. Mallika

UNIT – I

Operational Amplifier Fundamentals: Basic Opamp circuits, Op-amp parameters: input and output voltages, CMRR and PSRR, offset voltages and currents, input and output impedances, slew rate and frequency limitations.

Opamp as DC Amplifier: Biasing Opamps, direct coupled voltage follower, Non-inverting **a**mplifiers, inverting amplifiers, summing amplifiers, difference amplifiers, instrumentation amplifiers.

UNIT – II

Opamp as AC Amplifier: Opamp frequency response and compensation methods, capacitor coupled voltage follower, High input impedance capacitor coupled voltage follower, Capacitor coupled non-inverting amplifier, High input impedance capacitor coupled non-inverting amplifier, Capacitor coupled inverting amplifier, setting the upper cut off frequency, Capacitor coupled difference amplifier, use of single polarity voltage supply.

UNIT – III

Opamp Switching, Differentiating and Integrating Circuits: Voltage level detectors**:** Zero **c**rossing detector, level detector, voltage level monitor, Inverting Schmitt trigger circuit, Non-inverting Schmitt trigger circuit, Differentiating circuits, Integrating circuits, Log and Antilog amplifier, multiplier and divider.

Signal Processing Circuits using Opamp: Precision half-wave rectifiers, Precision full-wave rectifiers, Limiting circuits, Clamping circuits, Peak detectors, Sample and hold circuits.

UNIT – IV

Signal Generators: Triangular/Rectangular wave generator, Phase shift oscillator, Wien bridge oscillator, Monostable and Astable multivibrators.

Active Filters: Filter types and characteristics, first and second order low and high pass filter, first order two op-amp band pass and band reject filters.

UNIT – V

Applications of other linear ICs: Series opamp regulator, IC 723 general purpose regulator, 555 timer – basic timer circuit used as astable and monostable multivibrator, PLL operating principles.

D – A and A – D Converters: DAC/ADC specifications, weighted resistor DAC, R-2R DAC, Monolithic DAC, Flash type ADC, Counter type ADC, Successive Approximation ADC and Dual Slope ADC.

Textbooks:

1. David A. Bell, "Operational Amplifiers and Linear ICs", 3rd Edition, PHI/Pearson Education, 2011.
2. D. Roy Choudhury, Shail B. Jain, "Linear Integrated Circuits", 5th Edition, New Age International Publishers, 2018.

References:

1. Robert. F. Coughlin & Fred. F. Driscoll, "Operational Amplifiers and Linear Integrated Circuits", 6th Edition, PHI/Pearson Education, 2009.
2. Ramakant A. Gayakwad, "Op-Amps and Linear Integrated Circuits", 4th Edition, PHI/Pearson Education, 2004.

Course Outcomes (COs):

1. Discuss the construction, characteristics and parameter limitations of a basic Opamp. (POs – 1, 3, PSO – 1)
2. Design Opamp amplifier circuits. (POs – 1, 2, 3, PSO – 1)
3. Analyze and design switching and signal processing circuits using Opamp. (POs – 1, 2, 3, PSO – 1)
4. Demonstrate active filters and signal generators using Opamp.(POs – 1, 2, 3, 4, 12, PSOs – 1, 3)
5. Employ linear ICs in various applications. (POs – 1, 2, 3, 4, 12, PSOs – 1, 3)

FIELDS, LINES AND WAVES

Course Code: EC43 **Credits: 3:1:0**
Prerequisites: Engineering Physics **Contact Hours: 70**
Course Coordinator: Dr. B. Sujatha

UNIT – I

Electrostatics: Introduction to space co-ordinate system – Rectangular, cylindrical, spherical, infinitesimal length, area and volume, Gauss's law, Divergence, Maxwell's first equation (Electrostatics) and Divergence Theorem (only statement)

Energy and Potential: Energy expended in moving a point charge in an electric field, Definition of potential difference and potential, Potential field of a point charge, Potential gradient, Maxwell's second equation, Derivation of Poisson's and Laplace's equations, Construction and field analysis of coaxial line

UNIT – II

Magnetostatics: Ampere's circuital law, Curl, Stoke's theorem, Maxwell's third equation, Magnetic flux density, Scalar and magnetic potentials, Maxwell's fourth equation

Time-varying Fields and Maxwell's Equations: Faraday's law, Displacement current, Maxwell's equations in point form, Maxwell's Equations in integral form

UNIT – III

Uniform Plane Wave: Wave propagation in free space, Wave propagation in dielectrics, Poynting's theorem and wave power, Propagation in good conductors: Skin effect, Wave polarization (Qualitative treatment)

Waveguides: Rectangular waveguides, analysis of field components, cut off frequency, group and phase velocities, phase constants, dominant modes

UNIT – IV

Transmission Line Theory: Lumped element circuit model for a transmission line, wave propagation on a transmission line and general solutions of line, terminated lossless line, characteristic impedance, reflection coefficient, VSWR and impedance equation, special cases of terminated lossless line, Smith chart: construction and applications, conventional and graphical solution of line parameters.

UNIT – V

Impedance Matching and Tuning: Matching with lumped elements (L-section), Single stub tuning: shunt and series stubs using only Smith chart, Quarter wave transformer: bandwidth performance of the transformer, construction and field distribution of strip and micro-strip lines

Textbooks:

1. William H. Hayt Jr., John A. Buck, "Engineering Electromagnetics", 8th Edition, McGraw Hill Publications, 2010.
2. David M. Pozar, "Microwave Engineering", 3rd Edition, Wiley Publications, 2011.

References:

1. Mathew N. O. Sadiku, "Elements of Electromagnetics", 4th Edition, Oxford University Press, 2006.
2. John Ryder D, "Networks, Lines and Fields", Pearson India, 2015.

Course Outcomes (COs):

1. Analyze the concept of divergence, potential and energy density in electrostatic field distributions. (POs – 1, 2, 10, PSOs – 1, 3)
2. Explore the concept of magnetostatics and interpret Maxwell's equations for time varying fields. (POs – 1, 2, 10, 12, PSOs – 1, 3)
3. Interpret wave propagation through different media and rectangular waveguides. (POs – 1, 2, 4, 10, 12, PSOs –1, 3)
4. Evaluate parameters of transmission lines analytically and graphically. (POs – 1, 2, 3, 12, PSOs – 1, 3)
5. Employ Smith chart to design various impedance matching networks. (POs – 1, 2, 3, 12,. PSOs – 1, 3)

DIGITAL SIGNAL PROCESSING

Course Code: EC44 **Credits: 4:0:0**
Pre requisites: Signals and Systems **Contact Hours: 56**
Course Coordinator: Dr. C. G. Raghavendra

UNIT – I

Frequency Domain Sampling: Frequency domain sampling and reconstruction of discrete time signals.

Discrete Fourier Transform (DFT): Discrete Fourier Transform, DFT as a linear transformation, Relationship of DFT to other transforms, Properties of DFT.

UNIT – II

Linear Filtering: Use of DFT in linear filtering, Filtering long data sequences: overlap-save, overlap-add method.

Fast Fourier Transform (FFT) algorithms: Direct computation of DFT, Radix-2 FFT algorithm: Decimation-in-time algorithm, Decimation-in-frequency algorithm.

UNIT – III

FIR Filters: Design of FIR filters: Symmetric and anti-symmetric FIR filters, Design of linear phase FIR filters using windows and frequency sampling methods, FIR differentiators.

Structures for FIR Systems: Direct form structures, cascade form structures and lattice structures.

UNIT – IV

IIR Filters: Analog filter specifications, Classification of analog filters: Butterworth and Chebyshev approximations, Frequency transformations, Design of analog filters. Digital IIR filter design using impulse invariant technique, bilinear transformation, Matched z-transform methods.

IIR filter structures: Direct form (I and II), Cascade, Parallel, and Transposed structures.

UNIT – V

Architecture and Instruction set of TMS320C67x processor: Architecture, Pipelining, linear and circular addressing modes, Instruction sets, Assembler directives, Interrupts, Memory considerations, Fixed and floating point formats, Implementation of FIR and IIR filters.

Textbooks:

1. J. G. Proakis, D. G. Manolakis, "Digital Signal Processing: Principles, Algorithms and Applications", 4th Edition, Pearson Education Asia/Prentice Hall of India, 2014.
2. Rulph Chassaing, Donald Reay, "Digital Signal Processing and Applications with TMS320C6713 and TMS320C6416 DSK", 2nd Edition, Wiley India, 2014.

References:

1. S. K. Mitra, "Digital Signal Processing: A Computer based Approach", 4th Edition, McGraw Hill, 2013.
2. Sen M. Kuo, Woon-Seng S. Gan, "Digital Signal Processors – Architectures, Implementations and Applications", Pearson/Prentice Hall, 2005.
3. Emmanuel Ifeachor, Barrie W. Jervis, "Digital Signal Processing: A Practical Approach", 2nd Edition, Pearson Education, 2002.

Course Outcomes (COs):

1. Illustrate the importance of frequency domain analysis of LTI systems. (POs – 1, 2, 3, PSO – 3)
2. Apply DFT in linear filtering. (POs – 2, 3, 5, PSO – 3)
3. Design coefficients of FIR and IIR filters. (POs – 2, 3, 5, PSO – 3)
4. Develop digital structures for FIR and IIR filters. (POs – 2, 3, 5, PSO – 3)
5. Summarize architecture and instruction sets of TMS32067x processor. (POs – 2, 3, 5, PSO – 3)

CONTROL SYSTEMS

Course Code: EC45 **Credits: 3:1:0**
Prerequisites: Engineering Mathematics **Contact Hours: 70**
Course Coordinator: Mr. Sadashiva V Chakrasali

UNIT – I

Laplace Transformation: Basic theorems, Partial fraction expansion, Solution by Laplace transformation, transfer function and impulse response, Initial and Final value theorems, Convolution Integral, Solving linear circuits using Laplace transforms, Block diagrams and signal flow graph.

UNIT – II

Introduction: Examples of control systems, closed loop vs open loop control systems, classification of control systems.

Mathematical Modeling of Linear Systems: Analogous systems, translational and rotational mechanical systems.

UNIT – III

Time Response of Feedback Control Systems: Test input signals, time response of first and second order systems, Transient response specification of second order system, Steady state error and error constants. Applications: Design and analysis of second order system.

UNIT – IV

Stability Analysis: Concept of stability, Routh-Hurwitz criterion, Relative stability analysis, application of Routh stability criterion.

Root Locus Technique: Introduction, root-locus concepts, construction of root loci.

UNIT – V

Frequency Response Analysis: Introduction, Bode diagrams, assessment of relative stability using Bode plots.

Controllers: Classification of controllers, Brief analysis of different types of controllers.

Textbooks:

1. M. E Van Valkenburg, "Network Analysis". 3rd Edition, Pearson/Prentice Hall, 2006.
2. J. Nagrath and M. Gopal, "Control System Engineering", 6th Edition, New Age International Publishers, 2010.

References:

1. Ajit. K. Mandal, “Introduction to Control Engineering Modeling, Analysis and Design”, 2nd Edition, New Age International Publishers, 2012.
2. Dhanesh N. Manik, “Control Systems”, 1st Edition, Cengage Learning, 2012.

Course Outcomes (COs):

1. Solve basic theorems and transfer functions using Laplace transform.(POs – 1, 2, 5, PSO – 1)
2. Employ mathematical modeling techniques to determine the transfer function of a system. (POs – 1, 2, 5, PSO – 1)
3. Analyze the time response of first and second order systems. (POs – 1, 2, 5, PSO – 1)
4. Apply the concept of RH Criterion and root locus technique to determine the stability of a system. (POs – 1, 2, 4, 5, PSO – 1)
5. Interpret the frequency response using Bode’s plot and describe various controllers. (POs – 1, 2, 4, 5, PSO – 1)

MICROPROCESSORS

Course Code: EC46 **Credits: 3:0:0**
Prerequisites: Digital Design **Contact Hours: 42**
Course Coordinator: Mrs. Flory Francis

UNIT – I

Introduction to 8-bit 8085 Microprocessor: Architecture, addressing modes, memory, I/O interfacing.

8086 Microprocessor and its Architecture: Introduction, internal architecture of 8086, PSW, Real mode memory addressing.

UNIT – II

Addressing Modes: Data addressing mode, Program memory addressing mode, Stack memory addressing mode.

Instruction set of 8086: Data move, Arithmetic and Logic, Program control, Assembly language programming.

UNIT – III

Modular Programming: Assembler and linker, PUBLIC & EXTRN, Assembler directives, Programs using DOS interrupts, DOS function calls.

8086 Hardware Specifications: Pin outs and pin functions of 8086**,** clock generator 8284A, Bus buffering and latching, bus timing, READY and wait state, minimum mode versus maximum mode (Basic comparison only).

UNIT – IV

Memory, I/O and Peripheral Interfacing: Address decoding, memory interfacing for 8086, I/O port address decoding, Study of 8255 PPI and related programs.

Interrupts: Basic Interrupt Processing, Hardware Interrupts.

UNIT – V

Parallel Computers: Features of Parallel Computers, Structure of Parallel Computers, Classification of Parallel Computers, Vector Computers, Array Processors.

GPU Hardware Overview: PC Architecture, GPU Hardware**,** CPUs and GPUs.

Textbooks:

1. Ramesh Gaonkar, "Microprocessor Architecture, Programming and Applications with 8085", 6th Edition, Penram International Publishing, 2013.
2. Barry B Brey, "The Intel Microprocessors – Architecture, Programming and Interfacing", 8th Edition, Pearson Education, 2009.
3. V. Rajaraman, C. Siva Ram Murthy, "Parallel Computers – Architecture and Programming", Prentice Hall India Learning Private Limited, 2005.
4. Shane Cook, "CUDA Programming: A Developer's Guide to Parallel Computing with GPUs", 1st Edition, Morgan Kaufmann, 2012.

References:

1. A. K. Ray and K. M. Bhurchandi, "Advanced Microprocessor and Peripherals", 3rd Edition, Tata McGraw Hill, 2007.
2. Cameron Hughes, Tracey Hughes, "Professional Multicore Programming: Design and Implementation for C++ Developers", 1st Edition, Wrox Publishers, 2008.
3. Yu Cheng Liu, Glenn A Gibson, "Microcomputer Systems 8086/8088 Family, Architecture, Programming and Design", 2nd Edition, Prentice Hall of India, July 2003.

Course Outcomes (COs):

1. Explain the architecture of 8085 and 8086 processors. (POs – 1, 2, PSO – 2)
2. Develop assembly language programs for different addressing modes using instruction set of 8086 processor. (POs – 2, 3, 5, PSO – 2)
3. Describe 8086 hardware specifications and use modular programming for different applications. (POs – 2, 3, 5, PSO – 2)
4. Design interfacing circuits for 8086 processor. (POs – 2, 3, 5, PSO – 2)
5. Discuss parallel processing and GPU architecture. (POs – 1, 2, PSO – 2)

DSP AND CONTROL SYSTEMS LABORATORY

Course Code: ECL47 **Credits: 0:0:1**
Prerequisites: Engineering Mathematics **Contact Sessions: 14**
Course Coordinators: Mrs. H. Mallika

LIST OF EXPERIMENTS

Simulation Experiments

1. Generation of discrete and continuous time signals
2. Operations on discrete and continuous time signals
3. Convolution of discrete time signals and solution of difference equations
4. Design and implementation of FIR Filters (LP, HP, BP, BS) using window techniques
5. Design and implementation of analog and digital IIR filters (Butterworth and Chebyshev)
6. Representation of control systems by transfer function, partial fraction expansion and pole zero map
7. Block diagram reduction and system response
8. System analysis: Root locus, Bode plot
9. Simulink model of a control system and its response

Hardware Experiments

10. DFT, IDFT and Circular convolution
11. Response of discrete time systems
12. Filtering of noisy signal using FIR and IIR filter

Textbooks:

1. J. G. Proakis and Ingle, "Digital signal processing using MATLAB", 4th Edition, Cengage Learning, 2017.
2. Anoop K. Jairath and Saketh Kumar, "Control Systems – The state variable approach (Conventional and MATLAB)", 2nd Edition, Ane Books, 2013.

References:

1. Sanjit K. Mitra, "Digital Signal Processing", 4th Edition, Tata McGraw Hill, 2014.
2. Shailendra Jain, "Modeling and Simulation using MATLAB – Simulink", 2nd Edition, Wiley Publications, 2014.

Course Outcomes (COs):

1. Demonstrate the generation and various operations on signals. (POs – 1, 2, 5, PSO – 3)
2. Solve for the response of a discrete system. (POs – 1, 2, 3, 5, 8, 9, PSOs – 2,3)
3. Analyze the frequency response of digital filters. (POs – 1, 2, 3, 5, 8, 9, PSOs – 2,3)
4. Employ different models for control systems. (POs – 1, 2, 3, 4, 5, 9, PSO – 2)
5. Analyze the stability of control systems. (POs – 1, 2, 3, 4, 5, 9, PSO – 2)

MICROPROCESSORS LABORATORY

Course Code: ECL48 **Credits: 0:0:1**
Prerequisites: Digital Design **Contact Sessions: 14**
Course Coordinator: Mrs. Flory Francis

LIST OF EXPERIMENTS

Assembly Language Programs

1. Programs involving Data Transfer Instructions
   (i) Block move with and without overlapping
   (ii) Block move with overlapping
2. Programs involving Arithmetic Operations
   (i) Addition and Subtraction of N-bit multi precision numbers (N ≥ 32bits)
   (ii) Multiplication of 32- bits unsigned hexadecimal numbers
   (iii) Division of a 16-bit number by a 8-bit number
3. Programs involving Bit Manipulation Instructions.
   (i) 2 out of 5 codes
   (ii) Find the logical 1's and 0's in the given data
4. Find LCM, HCF and Factorial
   (i) Find LCM and HCF of given numbers
   (ii) Find factorial of a given number
5. Code Conversion
   (i) BCD to Hexadecimal
   (ii) Hexadecimal to BCD
   (iii) Addition and subtraction of two string ASCII digits
6. Programs involving Branch/Loop instruction
   (i) Sort the numbers in ascending order (bubble sorting)
   (ii) Find the smallest and largest 16-bit signed number in an array
7. Program for strings
   (i) Reverse a string
   (ii) Concatenation of input string with defined string
8. Program to search the occurrence of a character in the given string using DOS interrupt INT 21H
9. Interfacing Experiments
   (i) Delay calculation and generation of a square wave, triangular wave and stair case waveform using DAC. Display the waveform on a CRO
   (ii) Interfacing the stepper motor

Multi-core programming using OpenMP

10. C program to print "Hello World", from different cores
11. Add two arrays A and B using single and multi-core, and compare the processing time

Textbooks:

1. Barry B Brey, "The Intel Microprocessors – Architecture, Programming and Interfacing", 8th Edition, Pearson Education, 2009.
2. A. K. Ray and K.M. Bhurchandi, "Advanced Microprocessor and Peripherals", 3rd Edition, Tata McGraw Hill, 2007.
3. V. Rajaraman, C. Siva Ram Murthy, "Parallel Computers – Architecture and Programming", Prentice Hall India Learning Private Limited, 2005.

Course Outcomes (COs):

1. Write, compile and debug assembly language program using arithmetic instructions. (POs – 1, 2, 3, 5, PSO – 2)
2. Formulate assembly language programs for logical operations and code conversion. (POs – 1, 2, 3, 5, PSO – 2)
3. Develop programs using string and loop instructions. (POs – 1, 2, 4, 5, PSO – 2)
4. Write assembly language programs to interface stepper motor and DAC to 8086 microprocessor. (POs – 1, 2, 4, 5, PSO – 2)
5. Apply the concept of parallel computing to perform different operations. (POs – 1, 2, 4, 5, PSO – 2)